EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	598	716/3.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/12 20:31
L6	3834	thread and interfac$3 same programming and (attribute description rtl code hdl hard adj description adj language) and memory and interconnect$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/12 20:37
L7	2	1 and 6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/12 20:40
L8	582	716/16.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/12 20:42
L9	7	6 and 8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/12 20:42
S1	8394	message adj processing	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:43
S2	1371	attribute same thread and (program$5 configur$5 reconfigur$5)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 14:37
S3	19230	attribute same memory and (program$5 configur$5 reconfigur$5)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 14:37

EAST Search History

S4	37	S1 and S2 and S3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 14:38
S5	23540	(fpga pld cpld pla programmable adj device) and interface and memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 14:39
S6	2502689	design adjtool and implement$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 14:40
S7	5239	memory same interface same interconnection	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 14:40
S8	1851	interconnection with topology	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 14:41
S9	5	S4 and S5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 14:42
S10	35	S4 and S6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 14:44
S13	23	interfac$3 adj programming and design adj tool	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 14:58

EAST Search History

S14	5	interfac$3 adj programming and design adj tool and message adj processing	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 14:59
S15	5	interfac$3 adj programming and design adj tool and message adj processing and attribute	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:01
S16	124	interfac$3 same program$5 and design adj tool and message same processing and attribute and primitive	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:01
S17	59	interfac$3 same program$5 and design adj tool and message same processing and attribute and primitive and (thread parallel adj processing)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:03
S18	52	application same interfac$3 same program$5 and design adj tool and message same processing and attribute and primitive and (thread parallel adj processing)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:04
S19	41	application same interfac$3 same program$5 and design adj tool and message same processing and attribute and primitive and (thread parallel adj processing) and interconnect$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:05
S20	6	application same interfac$3 same program$5 and design adj tool and message same processing and attribute and primitive and (thread parallel adj processing) and interconnect$3 and (fpga pld cpld pla)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:05
S21	6	application and interfac$3 and program$5 and design adj tool and message same processing and attribute and primitive and (thread parallel adj processing) and interconnect$3 and (fpga pld cpld pla) and configur$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:07

EAST Search History

S22	4	application and interfac$3 and program$5 and design adj tool and message same processing and attribute and primitive and (multi adj2 thread parallel adj processing) and interconnect$3 and (fpga pld cpld pla) and configur$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:08
S23	4	interfac$3 and program$5 and design adj tool and message same processing and attribute and primitive and (multi adj2 thread parallel adj processing) and interconnect$3 and (fpga pld cpld pla) and configur$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:08
S24	13	interfac$3 and program$5 and message same processing and attribute and primitive and (multi adj2 thread parallel adj processing) and interconnect$3 and (fpga pld cpld pla) and configur$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:09
S25	2746	(first second) same attribute and thread and process$3 same (packet cell frame message)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:12
S26	1540	design adj tool same program$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:14
S27	7373	interconnect$3 same topology	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:13
S28	15215	memory same interface and thread	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:14
S29	2	S25 and S26 and S27 and S28	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:14

EAST Search History

S30	1611196	design adj tool amd program$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:14
S31	22	S25 and S27 and S28 and S30	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:15
S33	171	(fpga pld programmable adj logic) same programming adj interface	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:17
S34	168	(fpga pld programmable adj logic) same programming adj interface and (description attribute code hdl hardware adj description)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:19
S35	41	(fpga pld programmable adj logic) same programming adj interface and (description attribute code hdl hardware adj description) and (thread (multi parallel) adj2 process$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:20
S36	28	(fpga pld programmable adj logic) same programming adj interface and (description attribute code hdl hardware adj description) and (thread (multi parallel) adj2 process$4) and interconnect and interface	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:21
S37	454	(fpga pld programmable adj logic) and programming adj interface and (description attribute code hdl hardware adj description) and (thread (multi parallel) adj2 process$4) and interconnect and interface	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:21
S38	21695	(programming adj interface prgrammabel adj architecture) and (method tool apparatus)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:44

EAST Search History

S39	968707	(attribute code instruction language description) same (thread process)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:46
S40	12957	S38 and S39	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:46
S41	6100	S38 and S39 and interconnect$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:47
S42	6100	S38 and S39 and interconnect$3 and interface	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:47
S43	1219	S38 and S39 and interconnect$3 and interface and topology	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:48
S44	1171	S38 and S39 and interconnect$3 and interface and topology and memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:48
S45	173	S38 and S39 and interconnect$3 and interface and topology and memory and (pld cpld fpga programmable adj device)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:54
S46	210	S38 and S39 and interconnect$3 and interface and topology and memory and (pld cpld fpga programmable adj2 device)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:53

EAST Search History

S47	173	S38 and S39 and interconnect$3 and interface and topology and memory and (pld cpld fpga programmable adj device) and system	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 15:59
S48	6072	(thread multi adj2 processing) and interconnect$3 same memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 16:02
S49	215229	program$4 same interface	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 16:03
S50	1391477	(attribute feature description representation) same (thread process memory interface)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 16:24
S51	2844	S48 and S49 and S50	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 16:24
S52	1759	S48 and S49 and S50 and program same code	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 16:25
S53	414	S48 and S49 and S50 and program same code and primitive	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 16:25
S54	400	S48 and S49 and S50 and program same code and primitive and instruction	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 16:29

EAST Search History

S57	1	S48 and S49 and S50 and program same code and primitive and instruction and (FSM finite adj state) and design adj3 (method tool apparatus) and (fpga clpd pld pla)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 16:29
S58	145	S48 and S49 and S50 and program same code and primitive and instruction and (programmable adj device fpga cpd pla cpld)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 16:34
S59	143	S48 and S49 and S50 and program same code and primitive and instruction and (programmable adj device fpga cpd pla cpld) and configur$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 16:35
S60	293	(parallel multi) adj2 (process$3 thread instance execution) same design adj2 (tool method apparatus architecture)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 16:38
S61	86	(parallel multi) adj2 (process$3 thread instance execution) same design adj2 (tool method apparatus architecture) and memory and interface and interconnect$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 16:41
S62	67	(parallel multi) adj2 (process$3 thread instance execution) same design adj2 (tool method apparatus architecture) and memory and interface and interconnect$3 and model$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 16:57
S63	662	implement$5 with message adj process$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 16:58
S64	33	implement$5 with message adj process$3 and (thread)and memory and interconnect$3 and interfac$3 and (attribute description representation hdl verilog hardware adj description)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 17:06

EAST Search History

S65	5465	implement$5 same (multi adj2 process$3 thread)and memory and interconnect$3 and interfac$3 and (attribute description representation hdl verilog hardware adj description)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 17:07
S66	5468	implement$5 same (multi adj2 process$3 thread)and memory and interconnect$3 and interfac$3 and (attribute description rtl code hdl verilog hardware adj description)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 17:08
S67	2239	implement$5 with (multi adj2 process$3 thread)and memory and interconnect$3 and interfac$3 and (attribute description rtl code hdl verilog hardware adj description)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 17:08
S68	624	implement$5 with (multi adj2 process$3 thread)and memory same interconnect$3 same interfac$3 and (attribute description rtl code hdl verilog hardware adj description)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 17:09
S69	497	implement$5 with (multi adj2 process$3 thread)and memory same interconnect$3 same interfac$3 and (defin$3 describ$3 specif$6)same(attribute description rtl code hdl verilog hardware adj description)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 17:10
S70	136	implement$5 with (multi adj2 process$3 thread)and memory same interconnect$3 same interfac$3 and (defin$3 describ$3 specif$6)same(attribute description rtl code hdl verilog hardware adj description) and topology	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 17:10
S71	62	implement$5 with (multi adj2 process$3 thread)and memory same interconnect$3 same interfac$3 and (defin$3 describ$3 specif$6)same(attribute description rtl code hdl verilog hardware adj description) and topology and primitive	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 17:11

EAST Search History

S72	62	implement$5 with (multi adj2 process$3 thread)and memory same interconnect$3 same interfac$3 and (defin$3 describ$3 specif$6)same(attribute description rtl code hdl verilog hardware adj description) and topology and primitive and instruction	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 17:11
S73	62	implement$5 with (multi adj2 process$3 thread)and memory same interconnect$3 same interfac$3 and (defin$3 describ$3 specif$6)same(attribute description rtl code hdl verilog hardware adj description) and topology and primitive and instruction and set	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 17:12
S74	62	implement$5 with (multi adj2 process$3 thread)and memory same interconnect$3 same interfac$3 and (defin$3 describ$3 specif$6)same(attribute description rtl code hdl verilog hardware adj description) and topology and primitive and instruction and set and (FSM state adj machine state)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 17:13
S75	62	implement$5 with (multi adj2 process$3 thread)and memory same interconnect$3 same interfac$3 and (defin$3 describ$3 specif$6)same(attribute description rtl code hdl verilog hardware adj description) and topology and primitive and instruction and set and (FSM state adj machine state) and function$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 17:13
S76	62	implement$5 with (multi adj2 process$3 thread)and memory same interconnect$3 same interfac$3 and (defin$3 describ$3 specif$6)same(attribute description rtl code hdl verilog hardware adj description) and topology and primitive and instruction and set and (FSM state adj machine state) and function$3 and signal	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 17:17
S77	9584	defin$3 same (description code attribute) same thread and memory same interface and memory sane interconnect and (programming with interface) and primitive and topology and programmable adj device	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/01 17:24

EAST Search History

S79	632	716/17.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/02 10:09
S80	252	716/17.ccls. and memory and interconnect$3 and interface	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/02 10:11
S81	245	716/17.ccls. and memory and interconnect$3 and interface and program$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/02 10:12
S82	243	716/17.ccls. and memory and interconnect$3 and interface and program$5 and process$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/02 10:13
S83	150	716/17.ccls. and memory and interconnect$3 and interface and program$5 and process$3 and tool	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/02 10:16
S84	6	716/17.ccls. and memory and interconnect$3 and interface and program$5 and process$3 and tool and thread	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/02 10:19
S85	3	716/17.ccls. and memory and interconnect$3 and interface and program$5 and process$3 and tool and thread and message	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/02 10:43
S89	3	716/17.ccls. and memory and interconnect$3 and interface and program$5 and process$3 with message and tool and thread and (primitive library with (component cell)) and (run-time dynamic$4) and signal and debug$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/02 10:58

EAST Search History

S10 1	2401	message adj processing and interpret$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/12 13:54
S10 2	425	message adj processing and interpret$5 and XML	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/12 13:55
S10 3	11	message adj processing and interpret$5 and XML and interfac$3 adj program$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/12 18:05
S10 4	5	message adj processing and interpret$5 and XML and interfac$3 adj program$4 and (fpga programmable)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/12 13:56
S10 5	6	message adj processing and interpret$5 and XML and interfac$3 adj program$4 and design adj2 tool	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/12 14:12
S10 6	4	message adj processing and interpret$5 and XML and interfac$3 adj program$4 and design adj2 tool and thread	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/12 14:12
S11 3	20	state adj machine with circuit same thread	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/12 16:44
S11 4	7604	interpret$5 same (code language programming) same interface	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/12 19:28

EAST Search History

S115	253	interpret$5 same (code language programming) same interface and design adj tool	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/12 19:28
S116	253	interpret$5 same (code language programming) same interface and design adj tool and process$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/12 19:28
S117	135	interpret$5 same (code language programming) same interface and design adj tool and process$3 with (message)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/12 19:29
S118	241	interpret$5 same (code language programming) same interface and design adj tool and process$3 with (message data packet)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/12 19:29
S119	212	interpret$5 with (code language programming) same interface and design adj tool and process$3 with (message data packet)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/12 19:29
S120	59	interpret$5 with (code language programming) same interface and design adj tool and process$3 with (message data packet)and memory and thread	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/12 19:30
S121	57	interpret$5 with (code language programming) same interface and design adj tool and process$3 with (message data packet)and memory and thread and processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/12 19:30
S122	37	interpret$5 with (code language programming) same interface and design adj tool and process$3 with (message data packet)and memory and thread and processor and XML	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/12 19:31

EAST Search History

S123	6	interpret$5 with (code language programming) same interface and design adj tool and process$3 with (message data packet)and memory and thread and processor and (fpga pld programmable adj device)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/12 19:37
S124	57	interpret$5 with (code language programming) same interface and design adj tool and process$3 with (message data packet)and memory and thread and processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/12 19:37